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1 Compiling nested data-parallel programs for shared-memory multiprocessors

Siddhartha Chatterjee

July 1993 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 15 Issue 3

Full text available: pdf(4.17 MB) Additional Information: full citation, references, citings, index terms, review

**Keywords**: compilers, data parallelism, shared-memory multiprocessors

2 Computer simulation—discussion of the technique and comparison of languages

Daniel Teichroew, John Francis Lubin

October 1966 **Communications of the ACM**, Volume 9 Issue 10

Full text available: pdf(2.23 MB) Additional Information: full citation, abstract, references, citings

The purpose of this paper is to present a comparison of some computer simulation languages and of some of the packages by which each is implemented. Some considerations involved in comparing software packages for digital computers are discussed in Part I. The issue is obvious: users of digital computers must choose from available languages or write their own. Substantial costs can occur, particularly in training, implementation and computer time if an inappropriate language is chosen. More ...

3 Architecture: The architecture of the DIVA processing-in-memory chip

Jeff Draper, Jacqueline Chame, Mary Hall, Craig Steele, Tim Barrett, Jeff LaCoss, John Granacki, Jaewook Shin, Chun Chen, Chang Woo Kang, Ihn Kim, Gokhan Daglikoca

June 2002 **Proceedings of the 16th international conference on Supercomputing**

Full text available: pdf(295.98 KB) Additional Information: full citation, abstract, citings, index terms

The DIVA (Data IntensiVe Architecture) system incorporates a collection of Processing-In-Memory (PIM) chips as smart-memory co-processors to a conventional microprocessor. We have recently fabricated prototype DIVA PIMs. These chips represent the first smart-memory devices designed to support virtual addressing and capable of executing multiple threads of control. In this paper, we describe the prototype PIM architecture. We emphasize three unique features of DIVA PIMs, namely, the memory interf ...

**Keywords**: architecture, memory bandwidth, processing-in-memory

4 A Diagnostic Emulator for HEAO software development

Peter H. Beer, Kenneth J. Hupf

July 1976 **ACM SIGSIM Simulation Digest , Pr ceedings f the 4th symp sium n Simulati n of computer systems**, Volume 7 Issue 4

Full text available: pdf(701.56 KB) Additional Information: full citation, abstract, references, index terms

Diagnostic Emulation is the application of microprogramming to the emulation of an operational computer to support software development and verification for that computer. A conventional technique, Interpretive Computer Simulation (ICS), has been used for many years in support of such software development and verification efforts. The ICS method is becoming less cost effective. For the development of attitude control software for NASA's High Energy Astronomical Observatory (HEAO) diagnostic ...

5 A structural view of the Cedar programming environment

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann

August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4

Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

6 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young

March 1968 **Communications of the ACM**, Volume 11 Issue 3

Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

**Keywords**: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

7 Experience Using Multiprocessor Systems—A Status Report

Anita K. Jones, Peter Schwarz

June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2

Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

8 The network architecture of the Connection Machine CM-5 (extended abstract)

Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, Robert Zak

June 1992 **Proceedings of the fourth annual ACM symposium on Parallel alg rithms and architectures**

Full text available: pdf(2.00 MB) Additional Information: full citation, references, citings, index terms

9 Gilgamesh: a multithreaded processor-in-memory architecture for petaflops computing

Thomas L. Sterling, Hans P. Zima

November 2002 **Pr ceedings of the 2002 ACM/IEEE conference n Supercomputing**

Full text available: pdf(322.86 KB) Additional Information: full citation, abstract, references, citings, index terms

Processor-in-Memory (PIM) architectures avoid the von Neumann bottleneck in conventional machines by integrating high-density DRAM and CMOS logic on the same chip. Parallel systems based on this new technology are expected to provide higher scalability, adaptability, robustness, fault tolerance and lower power consumption than current MPPs or commodity clusters. In this paper we describe the design of *Gilgamesh*, a PIM-based massively parallel architecture, and elements of its execution mo ...

**Keywords**: Petaflops computing, Processor-In-Memory, data parallel processing, irregular applications, parallel architectures

10 Status report of the graphic standards planning committee

Computer Graphics staff

August 1979 **ACM SIGGRAPH Computer Graphics**, Volume 13 Issue 3

Full text available: pdf(15.01 MB) Additional Information: full citation, references, citings

11 The Clipper processor: instruction set architecture and implementation

W. Hollingsworth, H. Sachs, A. J. Smith

February 1989 **Communications of the ACM**, Volume 32 Issue 2

Full text available: pdf(4.67 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

12 System architectures for computer music

John W. Gordon

June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

13 An architectural framework for migration from CISC to higher performance platforms

Gabriel M. Silberman, Kemal Ebcioğlu

August 1992 **Pr ceedings of the 6th internati nal conference on Supercomputing**

Full text available: pdf(2.04 MB) Additional Information: full citation, abstract, references, citings, index terms

We describe a novel architectural framework that allows software applications written for a given Complex Instruction Set Computer (CISC) to migrate to a different, higher performance architecture, without a significant investment on the part of the application user or developer. The framework provides a hardware mechanism for seamless switching between two instruction sets, resulting in a machine that enhances application performance while keeping the same program behavior (from a user per ...

14 Technical reports

SIGACT News Staff

January 1980 **ACM SIGACT News**, Volume 12 Issue 1

Full text available: pdf(5.28 MB) Additional Information: full citation

15 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques

Luca Benini, Alberto Macii, Massimo Poncino

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

**Keywords**: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

16 OMP: a RISC-based multiprocessor using orthogonal-access memories and multiple spanning buses

K. Hwang, M. Dubois, D. K. Panda, S. Rao, S. Shang, A. Uresin, W. Mao, H. Nair, M. Lytwyn, F. Hsieh, J. Liu, S. Mehrotra, C. M. Cheng

June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing**, Volume 18 Issue 3

Full text available: pdf(1.96 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the architectural design and RISC based implementation of a prototype supercomputer, namely the Orthogonal MultiProcessor (OMP). The OMP system is constructed with 16 Intel 1860 RISC microprocessors and 256 parallel memory modules, which are 2-D interleaved and orthogonally accessed using custom-designed spanning buses. The architectural design has been validated by a CSIM-based multiprocessor simulator. The design choices are based on worst-case delay a ...

17 Curriculum recommendations for graduate professional programs in information systems

May 1972 **C mmunicati ns of the ACM**, Volume 15 Issue 5

Full text available: pdf(4.00 MB) Additional Information: full citation, references, citings

**Keywords**: education, information analysis, information systems development, management information systems, management systems, system design, systems analysis

**18** The structure of Cedar

Daniel C. Swinehart, Polle T. Zellweger, Robert B. Hagmann

June 1985 **Proceedings of the ACM SIGPLAN 85 symposium on Language issues in pr gramming environments**, Volume 20 , 18 Issue 7 , 6

Full text available: pdf(1.79 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing primarily on its overall structure: the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. We will emphasize the extent to which the Cedar language, with runtime support, has influenced the organization, comprehensibility, and stability of Cedar. Produced in the Computer Science Laboratory (CS ...

**19** Computer aided diagnostic design for electronic switching systems

Frank M. Goetz

June 1970 **Proceedings of the 7th workshop on Design automation**

Full text available: pdf(1.00 MB) Additional Information: full citation, abstract, references, index terms

With the advent of integrated circuitry, digital simulation has replaced physical fault insertion as the primary means for evaluating diagnostic tests. At Bell Laboratories, an improved version of the sequential analyzer was integrated into a data management system with a number of support programs. The system was used to evaluate the diagnostic program for a 32K core memory system under development for electronic switching system (ESS) applications. Important circuit design feedback was ob ...

**20** Linkers and Loaders

Leon Presser, John R. White

September 1972 **ACM Computing Surveys (CSUR)**, Volume 4 Issue 3

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1 **Memory-adaptive parallel sparse Cholesky factorization**
*Eswar, K.; Chua-Huang Huang; Sadayappan, P.;*
Scalable High-Performance Computing Conference, 1994. Proceedings of the , 23-25 May 1994
Pages:317 - 323

[Abstract] [PDF Full-Text (488 KB)] **IEEE CNF**

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